A High Performance 180 nm Generation Logic Technology

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Abstract

A 180 nm generation logic technology has been developed with high performance 140 nm L_{GATE} transistors, six layers of aluminum interconnects and low-ε SiOF dielectrics. The transistors are optimized for a reduced 1.3-1.5 V operation to provide high performance and low power. The interconnects feature high aspect ratio metal lines for low resistance and fluorine doped SiO_2 inter-level dielectrics for reduced capacitance. 16 Mbit SRAMs with a 5.59 μm^2 6-T cell size have been built on this technology as a yield and reliability test vehicle.

Introduction

Advanced logic technologies now lead the industry in requirements for transistor performance, interconnects and lithographic resolution. Transistor performance still dominates overall microprocessor speed and aggressive gate oxide and gate length scaling are needed to meet performance requirements. Power consumption is a growing consideration for microprocessors and continued supply voltage scaling is needed to meet power requirements. High performance microprocessors are also placing greater demands on interconnects. Interconnect density requirements can be met by scaling pitch and adding additional layers. Interconnect performance and power needs can be met by using mature aluminum technology with high aspect ratio metal lines for low resistance and low-e dielectrics for reduced capacitance. Increases in the amount of on-die cache memory on microprocessors is increasing the demand for small memory cells while not compromising the performance of logic circuits.

Transistors

Figure 1 illustrates the structure of the MOS transistors and isolations used in this technology. The transistor process flow starts with P-/P+ epitaxial silicon wafers followed by the formation of shallow trench isolation. N-wells are formed with deep phosphorous and shallow arsenic implants, while P-wells are formed with boron implants. The trench isolation is 530 nm deep to provide good intra- and inter-well isolation. The minimum N+ to P+ spacing is conservatively set at 560 nm, as demonstrated in Figure 2. Latchup is not observed even at spacings less than 560 nm due to the optimized well and trench structure and low 1.5 V supply voltage. The electrical gate oxide thickness is 3.0 nm as measured at 1.5 V under inversion conditions. As shown in Figure 3, the dielectric time to fail of the 3.0 nm gate oxide exceeds the requirement for 1.5V operation with allowed tolerances. Complementary-doped polysilicon is used to form surface-channel N-MOSFETs and P-MOSFETs. DUV lithography is used to pattern the polysilicon gate layer down to L_{GATE} dimensions of ~140 nm. Shallow source-drain extension regions are formed with arsenic for NMOS and boron for PMOS. Halo implants (boron and arsenic) are used in both cases for improved short channel characteristics. Low N+ and P+ junction capacitance values of 0.65 and 0.95 fF/μm^2 at 0 V are provided to improve performance and reduce active power. Sidewall spacers are formed with CVD Si_3N_4 deposition followed by etchback. $TiSi_2$ is selectively formed on polysilicon and source-drain regions with a nominal sheet resistance of 3 Ω/sq. Worse case sheet resistance of 5 Ω/sq is maintained for poly-Si line widths down to 110 nm as shown in Figure 4 for poly-Si lines with alternating N+ and P+ doping.

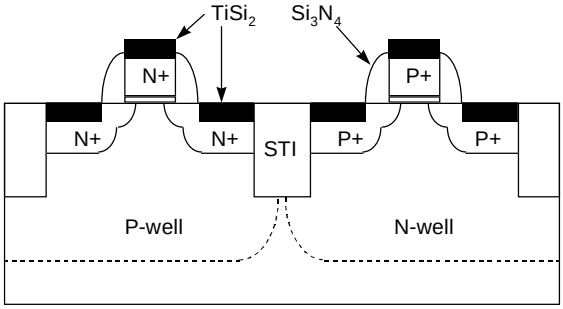

Fig. 1 Schematic cross-section of transistors

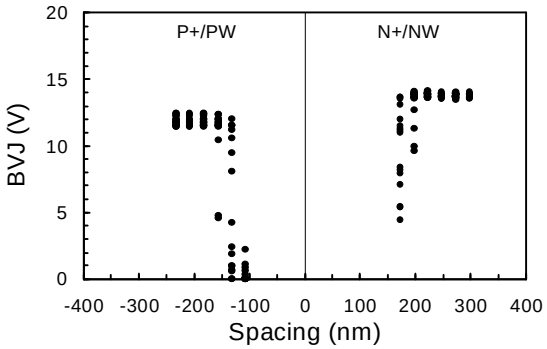

Fig. 2 P+/Pwell and N+/Nwell isolation

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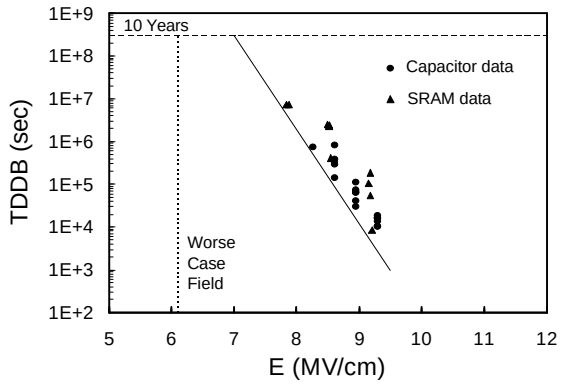

Fig. 3 3.0 nm gate oxide TDDB at 125C

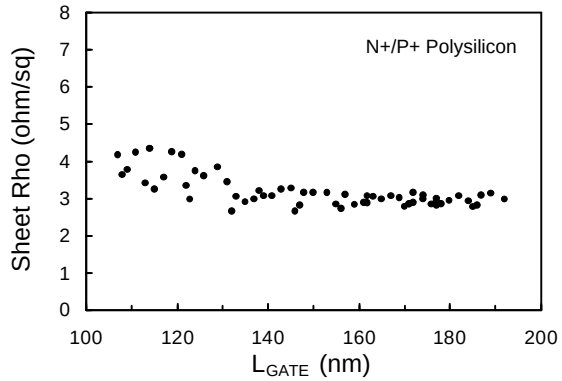

Fig. 4 $TiSi_2$ sheet resistance vs. polysilicon line width

MOSFET short channel characteristics are well controlled down to physical gate lengths (L_{GATE}) of 130 nm for NMOS and 150 nm for PMOS due to the use of a thin 3.0 nm gate oxide and careful optimization of source-drain extensions and halo implants. Saturation drive currents at 1.5 V are 0.94 mA/μm for NMOS and 0.42 mA/μm for PMOS at these L_{GATE} targets (Figure 5). Saturation transconductances are 860 and 430 mS/mm for NMOS and PMOS devices respectively. Subthreshold slopes for both NMOS and PMOS devices are less than 90 mV/decade at an I_{OFF} value of 3 nA/μm (Figure 6). Short channel threshold voltage roll-off characteristics are shown in Figures 7 and 8. Threshold voltages at 1.5 V drain bias are 0.30 V for NMOS at 130 nm L_{GATE} and -0.24 V for PMOS at 150 nm L_{GATE}. NMOS and PMOS drive current vs. off current characteristics are shown in Figure 9. These results are better than any previously published bulk [1-3] or SOI [4-5] devices. Figure 10 shows inverter gate delay vs. gate length for unloaded ring oscillators (fan out = 1) operating at 1.3 V and 1.5 V and at room temperature. The delay per stage at minimum gate lengths is <13 psec at 1.3 V and <11 psec at 1.5 V. These fast delays are obtained even with a conservative I_{OFF} value of 3 nA/μm.

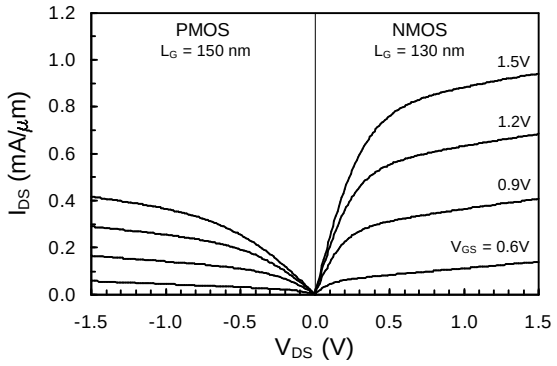

Fig. 5 MOSFET I-V curves

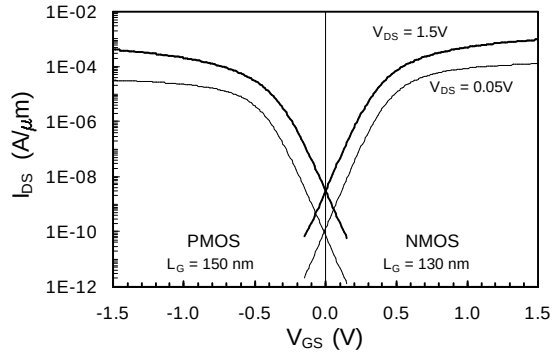

Fig. 6 MOSFET subthreshold curves

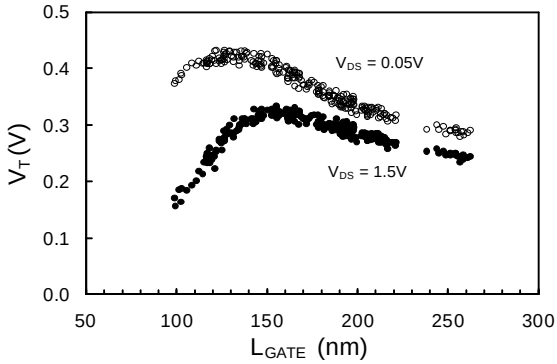

Fig. 7 NMOS threshold voltage vs. gate length

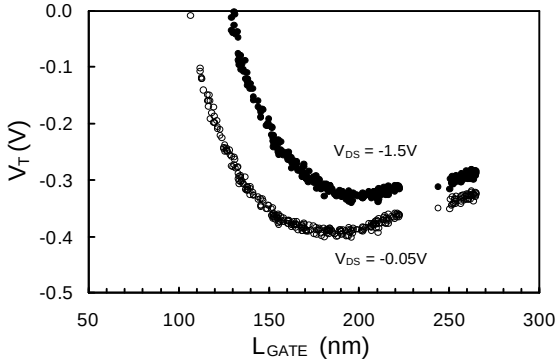

Fig. 8 PMOS threshold voltage vs. gate length

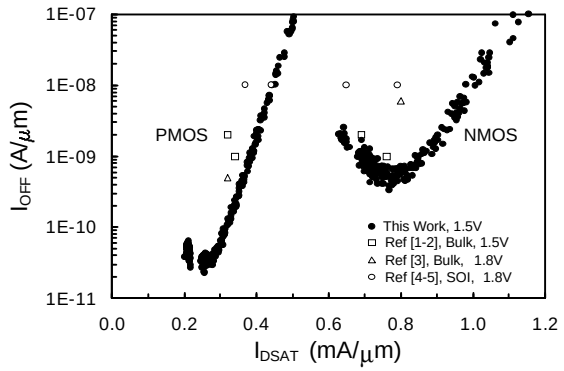

Fig. 9 MOSFET drive current vs. off current

LAYER	PITCH	THICK	A.R.
Isolation	520	530	-
Polysilicon	480	250	-
Metal 1	500	480	1.9
Metal 2, 3	640	700	2.2
Metal 4	1080	1080	2.0
Metal 5	1600	1600	2.0
Metal 6	1720	1720	2.0
	nm	nm	

Table 1 Layer pitch, thickness and aspect ratio

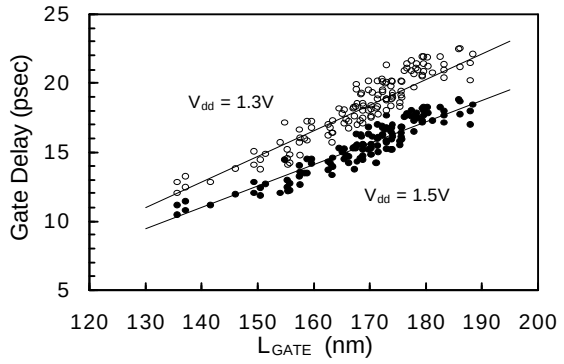

Fig. 10 Inverter gate delay per stage vs. L_{GATE}, FO=1

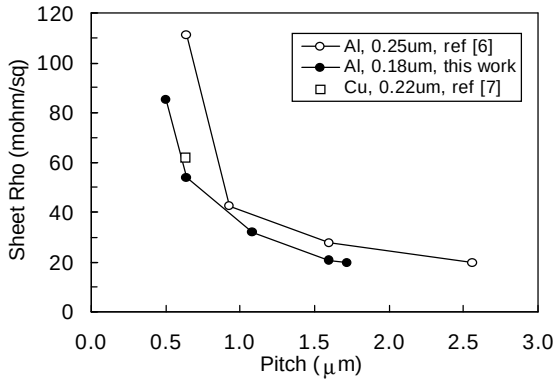

Fig. 11 Interconnect sheet resistance vs. pitch

Interconnects

Six metal layers are used to address the increasing importance of interconnects to microprocessor performance and density. Contacts and vias are all filled with tungsten plugs formed with PVD Ti/CVD TiN adhesion layers and blanket tungsten deposition followed by chemical-mechanical polish. The metal stack is Ti/Al-Cu/Ti/TiN which provides low line resistance, good electromigration and low via resistance. The pitches and thicknesses of the interconnect layers are summarized in Table 1. Aggressive metal aspect ratios (thickness/width) are used to provide low interconnect resistance at tight pitches. Figure 11 summarizes a study that compares the metal sheet resistance vs. pitch for this technology to Intel's previous 0.25 μm technology [6] and to a recent copper interconnect technology [7]. For a given pitch, this aluminum technology has a lower sheet rho than any reported to date. M1 pitch is tight for optimal density as a local interconnect and for a small 6-T SRAM cell size. M2 and M3 use an intermediate pitch to optimize both density and performance. M4, M5 and M6 use increased pitches and thicknesses to optimize for low resistance and for fast signal propagation. The process uses a total of 21 masking layers, combining DUV for critical layers and I-line for non-critical layers.

The inter-level dielectric between polysilicon and metal 1 is PSG planarized by chemical-mechanical polish. The inter-level dielectric between the metal layers is HDP oxide doped with 5.5% fluorine and planarized by chemical-mechanical polish. Fluorine is added to SiO_2 to reduce dielectric constant and improve interconnect performance [8, 9]. The use of SiOF as an inter-level dielectric reduces the dielectric constant to 3.55 compared to 4.10 for undoped HDP and PTEOS oxides. Metal interconnect intensive ring oscillators were used to quantify the speed benefit of SiOF ILD. A M2/M3/M4 sandwich structure with interdigitated M3 lines sandwiched between planes of M2 and M4 was used to test total M3 line capacitance. A M3 isolated structure with interdigitated M3 lines and no M2 or M4 planes was used to test lateral M3-M3 line capacitance. As shown in Table 2, ring oscillator frequencies showed an increase of 16% for the sandwich structure and 14% for the isolated structure with the use of SiOF. The fact that SiOF improves the performance of both isolated and sandwich structures indicates that it is effective in improving both in-plane and out-of-plane capacitance. The ILD capacitance reduction is important for both improving interconnect performance and for reducing chip active power. A cross-section of the interconnects used on this process is shown in Figure 12.

	Dielectric Constant	M2/M3/M4 Sandwich	M3 Isolated
HDP SiO_2	4.10	--	--
PTEOS	4.10	+0%	+5%
HDP SiOF	3.55	+16%	+14%
	ε	RO incr.	RO incr.

Table 2 ILD effects on ε and ring oscillator frequency

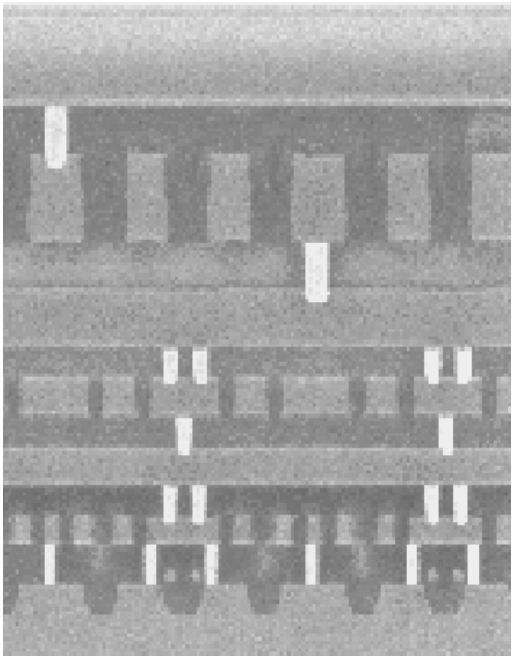

Fig. 12 Process cross-section

16 Mbit SRAM

A 16 Mbit CMOS SRAM has been designed and fabricated on this technology with high yields. This SRAM is used as a yield and reliability test vehicle during process development and to test and refine the SRAM cell and support circuitry to be used in logic products. A 6-T memory cell is used with dimensions of 2.22 x 2.52 μm and an area of 5.59 μm^2. Figure 13 shows top views of the cell after polysilicon and metal 1 layer processing. Three layers of metal are needed to make the SRAM cell functional: M1 for internal hook-ups and V_{DD} strapping, M2 for bitlines and V_{SS} strapping, and M3 for wordline strapping. M4, M5 and M6 are added to the cell as redundant V_{DD}, V_{SS} and wordline straps to make the 16 Mbit SRAM an appropriate process development vehicle for a 6-layer logic technology. The 16 Mbit SRAM die size is 207 mm^2 and a die photo is shown in Figure 14. The SRAM operates at >900 MHz at 1.5 V.

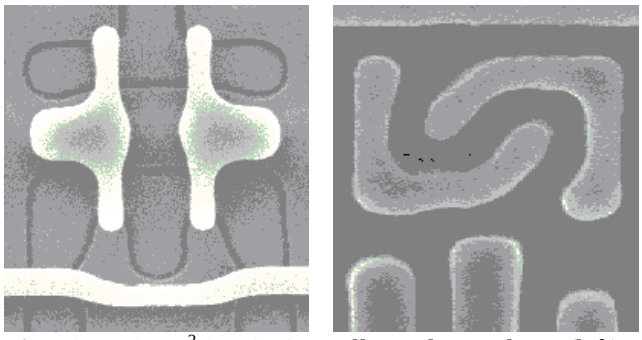

Fig. 13 5.59 μm^2 6-T SRAM cell at poly gate layer (left) and metal 1 (right)

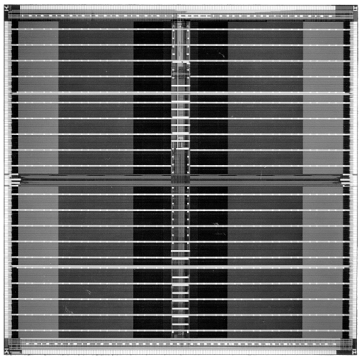

Fig. 14 16 Mbit SRAM die photo, 14.25 x 14.55 mm

Conclusion

A 180 nm generation logic technology has been developed and demonstrated with high performance, reduced power transistors. Aluminum interconnects with low-ε SiOF dielectrics are used to meet interconnect density and performance requirements. The technology yield and performance capabilities have been demonstrated on a 16 Mbit SRAM which operates at >900 MHz..

Acknowledgment

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